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OPTICAL MEMORY AND LOGIC USING CROSS-SWITCHES

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BACKGROUND

The present invention relates generally to optical memory, and more particularly, to improved optical memory and logic using cross-switches.

Conventional all-optical memory approaches include technologies based on fiber delay lines, semiconductor optical amplifiers, quantum dots, self-electro-optic effect devices, and gain-coupled lasers.

Fiber delay lines are not randomly accessible nor are they very small. Semiconductor optical amplifiers, quantum dots, self-electro-optic effect devices and gain-coupled lasers all require electronic biasing. It would be advantageous to have optical memory and logic that improves upon these conventional approaches.

It is an objective of the present invention to provide for improved optical memory and logic employing cross-switches. It is also an objective of the present invention to provide for an all-optical asynchronous binary memory cell and logic functions implemented with optically induced total internal reflection X-junction waveguide optical switches.

SUMMARY OF THE INVENTION

To meet the above and other objectives, the present invention provides for optical memory and logic that employs cross-switches to implement all-optical asynchronous binary memory cell and logic functions. The optical memory and logic functions are implemented with optically induced total internal reflection cross-junction waveguide optical switches.

The binary cell is a building block for a programmable all-optical random access memory (AORAM) device. AORAM devices enable circuits and networks that require optical buffers.

The present invention provides for all-optical random access memory (buffer) and all-optical logic, which is necessary for all-optical computing and all-optical networks. The present invention uses optically-induced total internal reflection to achieve all-optical switching, logic and memory functions. Devices based on the cross-switches employed in the present invention require no electronic biasing and are very compact. The present all-optical memory cell is randomly accessible.

BRIEF DESCRIPTION OF THE DRAWINGS

The various features and advantages of the present invention may be more readily understood with reference to the following detailed description taken in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements, and in which:

Fig. 1 illustrates an exemplary cross-switch in accordance with the principles of the present invention when observed at an oblique angle;

Fig. 2 illustrates an equivalent optical analog circuit model for the cross-switch device shown in Fig. 1;

Fig. 3 illustrates an optical equivalent digital circuit of the device shown in Fig. 1;

Fig. 4 illustrates an exemplary logic circuit implemented in accordance with the present invention;

Fig. 5 illustrates a proposed optical digital equivalent schematic corresponding to Fig. 4;

Fig. 6 illustrates an electrical digital equivalent circuit for an asynchronous binary memory cell;

Fig. 7a illustrates an equivalent electrical digital circuit of a single cross-switch device;

Fig. 7b illustrates a schematic of the device depicted in Fig. 7a;

Fig. 8a illustrates an electrical digital schematic of a 3-port AND gate with the corresponding truth table;

Fig. 8b illustrates a cross-switch implementation of the 3-port AND gate shown in Fig. 8a;

Fig. 9 illustrates an equivalent digital electrical diagram along with the corresponding truth table of a S-R (set/reset) latch;

Fig. 10a illustrates an electrical digital representation of a 2-port NAND gate along with its corresponding truth table;

Fig. 10b illustrates a cross-switch embodiment of the 2-port NAND gate shown in Fig. 10a;

Fig. 11 illustrates cross-coupled optical NAND gates that are combined to form an all-optical S-R latch; and

Fig. 12 illustrates an all-optical memory cell that combines the cross-switch logic gates shown in Figs. 7b, 8b and 11.

DETAILED DESCRIPTION

Referring to the drawing figures, Fig. 1 illustrates an exemplary cross-switch 10 in accordance with the principles of the present invention when observed at an oblique angle. The exemplary cross-switch 10 may be used to implement an all-optical, asynchronous binary storage cell, wherein the cross-switch 10 employs optically induced total internal reflection. The binary cell is a building block for a programmable all-optical random access memory (AORAM) device, which enables circuits and networks that require optical buffers.

In order to simplify the definition of a binary memory cell, several logic gates and their functions are described below. Corresponding all-optical equivalent logic gates using cross-switches are also described. As defined herein, the term "all-optical" refers to the directing of optical data signals as a result of optical control signal inputs without the need for conversions between optical and electrical domains.

The all-optical switch 10 is referred to a cross-switch 10. A general understanding of the cross-switch 10 is provided in US Patent Application Serial No. 10/264,609, filed October 4, 2002, and entitled, "Optically Induced Total Internal Reflection X-Junction Waveguide Optical Switch, Network and Optical Switching Method", which is assigned to the assignee of the present invention. The contents of this application are incorporated herein in its entirety by reference.

Referring to Fig. 1, the primary function of the exemplary cross-switch 10 is to direct incoming guided light from a first input port (Input 1) to one of two output ports (Output 1 or Output 2), based on the presence or absence of light from a second input port (Input 2, or pump port).

The exemplary optical switch 10 shown in Fig. 1 has a 1-input-by-2-output (1x2) port configuration. Activation of the cross-junction waveguide switch 10 uses a high intensity pump beam 17 (comprising an optical carrier), which may be provided by a laser 18. such as a vertical cavity surface emitting laser 18, for example.

As is shown in Fig. 1, the exemplary optical switch 10 comprises a plurality of single mode optical ridge waveguides 11 intersecting at an angle between the waveguides 11 at a cross-junction (or X-junction). The ridge waveguides 11 have a two-dimensional effective refractive index n_r, while cladding in a surrounding field area has two-dimensional refractive index n_c such that $n_r > n_c$. An optical signal propagates with a mode effective index n_m, which is a weighted average of n_r and n_c. An interaction region 15 illustrated by the dashed box in the center of the X-junction is where optical switching action occurs. The interaction region 15 may be activated by a high intensity pump beam 17 that illuminates the top-side of the interaction region 15. These aspects of the optical switch 10 are discussed in detail in the above-referenced US Patent Application.

Fig. 2 shows an equivalent optical analog circuit model of the cross-switch 10 illustrated in Fig. 1. The cross switch 10 is represented by a switch 21. The implied functionality is as follows. If Input 2 is active, then light from Input 1 is directed to Output 1. If a signal from Input 2 is absent, then incoming light from Input 1 exits via Output 2. In essence, Input 2 is a control port for an optically actuated 1x2 optical cross-switch 10.

For binary data (i.e., digital or on-off keyed signals), the optical equivalent circuit of the cross-switch 10 shown in Fig. 3 is applicable, where standard digital element representations for an inverter 22 and an AND gate 23 are used. The associated truth table is shown at the right of the cross-switch 10. The Boolean logic variables Y and A are substituted for the two ports, Input 1 and Input 2, respectively. The following conditions apply: no output signal results if Y = 0 (i.e., no incoming signal light); if Y = 1 (i.e., light constantly applied to Input 1), then Output 1 provides a copy of a digital input to A, while Output 2 simultaneously produces the digital complement of A. The latter condition is key to logic gate implementations using the cross-switch 10, and is further illustrated in Fig. 4.

Fig. 4 shows that an example digital optical signal is applied to Input 2 and a continuous wave (CW) optical signal is applied to Input 1 to effect a copy and complement of A. In order to simplify future schematic representations, Fig. 5 is used throughout the remainder of this description to describe the Y = 1 condition optical digital equivalent circuit. In practice, the Y = 1 condition can be obtained by coupling a CW laser diode directly to Input 1 of the cross-switch 10.

An electrical digital equivalent circuit for an asynchronous binary memory cell 30 is shown in Fig. 6. This memory cell 30 is adapted from a circuit described by M. Morris Mano, in Computer Engineering: Hardware Design, Prentice-Hall, New Jersey, 1988.

The memory cell 30 is subdivided into six sections to aid in demonstrating fundamental building blocks: sections 31 and 34 (sections I and VI) provide a copy and a digital complement of the input signal; sections 32, 33 and 35 (sections II, III and V) are 3-port AND gates 32, 33, 35; section 34 (section IV) is an S-R latch 34. Optical implementations for each of the building blocks is described below.

The equivalent electrical digital circuit of Sections 31 and 34 (sections I and VI) is shown in Fig. 7a. For digital optical signals, a single cross-switch 10 provides at its outputs, both a copy of, and the complement of, the signal applied to Input 2 (assuming that Input 1 = 1). Therefore, the cross-switch 10 implementation of Fig. 7a is simply a single cross-switch device, the schematic of which is depicted in Fig. 7b, with a CW laser explicitly shown at Input 1 to represent the Y = 1 condition.

Sections II, III and V represent 3-port AND gates 32, 33, 35, respectively. The electrical digital schematic of the 3-port AND gates 32, 33, 35 is shown in Fig. 8a, along with its corresponding truth table. Note that a '1' at the output is only possible if all input ports are set 'high' (A = B = C = 1).

The cross-switch implementation of the 3-port AND gate function is shown in Fig. 8b. It is comprised of three cascaded cross-switches 10, each with its own control signal. The complemented output is not used, and is therefore terminated. The second switch 10 (with B input control) receives a switchable incoming light signal only if one is passed to it from the first switch 10 (with A input control). Similarly for the third cascaded switch 10 (with C input control), light must first be passed through the first and second switches 10. Thus, the AND function is developed

It is conceivable to string an indefinite number of switches in order to create an N-port optical AND gate 32, 33 and 35. The timing of the control signals account for potentially different optical path lengths and the signal time-of-flight.

Section 34 (IV) is the S-R (set/reset) latch 34. The equivalent digital electrical diagram along with the corresponding truth table is shown in Fig. 9. This particular implementation uses two cross-coupled NAND gates 38. Thus, in order to demonstrate an optical S-R latch 34, an equivalent cross-switch implementation of a NAND gate 38 is first required. Fig. 10a shows the electrical digital representation of a 2-port NAND gate 38, along with its corresponding truth table. The cross-switch version is illustrated in Fig. 10b. This circuit is very similar to the AND gate 32, 33, 35 described previously (Fig. 8b), except that the complementary output of the final cascaded device (with control input B) is used to provide the NAND signal. Likewise, an N-port NAND gate 38 can be created from N-cascaded cross-switches 10. The cross-coupled optical NAND gates 38 may be combined to form the all-optical S-R latch 34 shown is Fig. 11.

As for signal levels, when the output of one gate/switch/section is used as the input/pump control signal for a subsequent gate/switch/section, it is conceivable that the optical power requires boosting between these stages. If required, optical amplifiers may be inserted between stages in order to increase the optical signal level. Adding such amplification does not change the principle operation of the logic gates described herein.

Finally, substituting all the cross-switch logic gate implementations shown in Figs. 7b, 8b and 11 for their corresponding sections in the memory cell shown in Fig. 6, produces an all-optical binary memory cell 39 shown in Fig. 12. Fig. 12 thus shows an all-optical binary memory cell 39 using the cross-switches 10.

Thus, improved optical memory and logic using cross-switches have been disclosed. It is to be understood that the described embodiments are merely illustrative of some of the many specific embodiments which represent applications of the principles of the present invention, such as open stub reflection circuits and logic pulse generation circuits, for example. Clearly, numerous and other arrangements can be readily devised by those skilled in the art without departing from the scope of the invention.